IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Confirmation No. 4145

David C. CHAPMAN Group Art Unit No.: 2825

Serial No.: 09/421,437 Examiner: A.M. Thompson

Filed: October 19, 1999

For: APPROACH FOR ROUTING AN INTEGRATED CIRCUIT

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

REPLY BRIEF

Sir:

This Reply Brief is submitted in response to The Examiner's Answer mailed on June 4, 2002.

I. INTRODUCTION

Applicant believes that the following comments will be helpful to the Board of Patent Appeals and Interferences in making its decision regarding the application referenced above.

II. CLAIMS 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 AND 67: THE EXAMINER HAS IMPROPERLY READ LIMITATIONS FROM THE SPECIFICATION INTO THE CLAIMS

In the Examiner's Answer, the Examiner has improperly read limitations from the specification of the present application into the claims. Specifically, the Examiner has identified

alleged similarities between the "simple routing indicator" described on page 27 of the present application and *Adler* in an attempt to support the rejection of all Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 based on *Adler* when in fact the "simple routing indicator" is not even introduced in the claims until Claim 13.

The "simple routing indicator" identified by the Examiner is completely different than the "routing indicators" recited in Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67. These claims require "one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices." As set forth at page 27 of the present application, "a simple routing indicator is used generally to control whether changes are made to surrounding geometry during detailed routing of a new wire." When the simple routing indicator is asserted during detailed routing, wires are routed around obstacles, instead of allowing the obstacles or surrounding geometry to be modified. Routing around obstacles is "simple routing" relative to routing that includes the modification of obstacles or surrounding geometry.

As described on page 27 of the present application, making changes to layout geometry during routing can have undesirable effects on fabrication and performance. "For example, clipping the corner of a contact enclosure makes the contact enclosure more sensitive to misalignment and may reduce fabrication yield. Similarly, clipping the corner of a transistor island or adjusting a source/drain contact increases source/drain resistance and thus slows the integrated circuit" (page 27 of present application). Accordingly the present invention allows geometry modification to be disabled using a "simple routing indicator" to accommodate situations where it is desirable to mitigate possible side effects attributable to modifying layout geometry.

Thus, the Applicant submits that the discussion contained on pages 15-17 of the Examiner's Answer related to the "simple routing indicator" is completely irrelevant to the rejection of Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 over *Adler*, since this limitation is not found in the claims. Accordingly, the Applicant requests that the Honorable Board of Patent Appeals and Interferences give no weight to the Examiner's discussion of the "simple routing indicator."

III. CLAIMS 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 AND 67 ARE PATENTABLE OVER *ADLER* BECAUSE *ADLER* DOES NOT TEACH OR SUGGEST ROUTING AN INTEGRATED CIRCUIT USING "ROUTING INDICATORS THAT SPECIFY A SET OF ONE OR MORE PREFERABLE INTERMEDIATE ROUTING LOCATIONS THROUGH WHICH A ROUTING PATH IS TO BE LOCATED" AS REQUIRED BY THE CLAIMS

The Applicant would like to reiterate that the steps of "determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices" and "determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria," both of which are explicitly required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67, are not in any way taught or suggested by *Adler*.

In *Adler*, the 32 bit integer value associated with a grid point contains bits that specify whether it is forbidden to extend a wavefront search in a particular direction from the grid point. Specifically, "bits 21 to 29 store information whether it's forbidden to extend the wave from the current grid point to the neighboring grid points" (*Adler*, Section 3.1). In the example depicted in Figure 6 of *Adler*, bits 21 to 29 of the integer value associated with grid point *a* are set to indicate that the wave cannot be propagated from point *a* into grid points *b*, *c*, *d*, *e* or *f*. Thus, suppose that the bits associated with the directions towards grid points *b* and *c* are set. That would mean that starting from point a, valid directions for extending the wavefront search would be towards grid points *d*, *e* or *f*. In the Examiner's Answer, the Examiner states "*Adler*'s use of the routing indicator to forbid wiring in a certain location, thereby forcing routing in an alternate area indicates a routing preference for some alternate location." The 32 bit integer value, however, only indirectly specifies which directions are available for searching, and does not contain any additional information that indicates which of the available directions should be chosen for routing. Thus, the 32 bit integer value of *Adler* does not indicate a routing preference, as asserted by the Examiner, since in this example, all of the remaining three directions (*d*, *e* and *f*) are equal available choices and will be searched. Accordingly, the Applicant submits that the use of "routing indicators that specify a set of **one or more preferable intermediate routing locations** through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices," as required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67, is not in any way taught or suggested by *Adler* since the 32 bit integer value of *Adler* does not indicate "one or more preferable intermediate routing locations through which a routing path is to be located."

Applicant therefore respectfully submits that the rejection of Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 over *Adler* cannot be sustained, since several limitations required by these claims are not in any way taught or suggested by *Adler*.

IV. CONCLUSION

Based on the foregoing, it is respectfully submitted that after consideration of the Examiner's Answer, that the rejection of Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 under 35 U.S.C. § 103(a) over *Adler* still lacks the requisite factual basis.

Respectfully submitted,

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on August 5, 2002 by Sheila Severinghaus